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ART UNIT	**PAPER NUMBER**
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,453	JOSHI ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 33-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 31-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-19, and 31-45 have been considered but are moot in view of the new ground(s) of rejection.

Withdrawal of Finality

The previous office action put this application under FINAL rejection. That holding is hereby withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 5, and 7 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Shibata, US Patent 6,461,890.

Shibata (Figures 5 & 6) teaches a wafer-level chip scale package, comprising:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate.

Regarding claim 2, Shibata teaches at least one conductive particle is located between the stud bump and the bond pad (figure 6).

With respect to claim 4, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

As to claim 5, Shibata teaches the chip contains an integrated circuit in communication with a chip pad (7, 44+).

In re claim 7, Shibata, which teaches the bump is made of gold (7, 45+), teaches the package does not contain any solder paste.

Claims 37, 38, and 40 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Shibata, US Patent 6,461,890.

Shibata (Figures 5 & 6) teaches an electronic apparatus containing a wafer-level chip scale packaged semiconductor device, comprising:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate.

Regarding claim 38, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

With respect to claim 40, Shibata, which teaches the bump is made of gold (7, 45+), teaches the packaged device does not contain solder paste.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, as applied to claim 1 above, and further in view of Kaneda et al., US Patent 6,223,429.

Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, as applied to claim 1 above, and further in view of Applicant's admitted prior art APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, as applied to claim 1 above.

Regarding claim 8, while Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging – Part II, 1997, pp II-207. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

With respect to claim 9, while Shibata fails to teach the stud bump is a coined stud bump, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a coined stud bump in the invention of Shibata because the use of a stud bump or a coined stud bump are equivalent. A skilled artisan knows that each are commonly known and used bumps to interconnect a die to a substrate, as taught by Lau, Flip Chip Technologies, 1996, pp. 129-131. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960);

Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

As to claim 10, while Shibata fails to teach the chip does not contain a chip pad overlying an integrated circuit (IC), this is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)). Placement of the chip pad relative to the IC is known to a skilled artisan since placing it away from the chip pad protects the IC from the heat and pressure put upon the pad.

Claims 11, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata (figure 5) teaches a wafer-level chip scale package, comprising:

a chip [10] containing a stud bump [11];

a substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate with at least one conductive particle contacting both the stud bump and the bond pad.

While Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging

Handbook: Semiconductor Packaging – Part II, 1997, pp II-207. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Further, Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Regarding claim 12, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

With respect to claim 14, Shibata, which teaches the bump is made of gold (7, 45+), teaches the packaged device does not contain solder paste.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429, as applied to claim 11 above, and further in view of APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Claims 15, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata (figure 5) teaches a wafer-level chip scale package, comprising:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate with at least one conductive particle contacting both the stud bump and the bond pad.

While Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging – Part II, 1997, pp II-207. The substitution of one

known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Further, Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Regarding claim 16, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

With respect to claim 18, Shibata, which teaches the bump is made of gold (7, 45+), teaches the packaged device does not contain solder paste.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429, as applied to claim 15 above, and further in view of APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata (figure 5) teaches an electronic apparatus containing a packaged semiconductor device without solder paste (7, 45+), the device comprising:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] contacting both the chip and the substrate.

Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because

Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Claims 33, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata teaches a wafer-level chip scale packaged semiconductor device, the device comprising:

a chip [10] containing a stud bump [11];

a substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate.

Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Regarding claim 34, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

With respect to claim 36, Shibata, which teaches the bump is made of gold (7, 45+), teaches the packaged device does not contain solder paste.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429, as applied to claim 33 above, and further in view of APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429, as applied to claim 37 above, and further in view of APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Claims 41, 42, 44, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429.

Shibata (figure 5) teaches a wafer-level chip scale package without solder paste (7, 45+), comprising:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate, wherein a conductive particle contacts both the stud bump and the bond pad.

Shibata fails to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Regarding claim 42, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

With respect to claim 44, while Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging – Part II, 1997, pp II-207. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

As to claim 45, while Shibata fails to teach the stud bump is a coined stud bump, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a coined stud bump in the invention of Shibata because the use of a stud bump or a coined stud bump are equivalent. A skilled artisan knows that each are commonly known and used bumps to interconnect a die to a substrate, as taught by Lau, Flip Chip Technologies, 1996, pp. 129-131. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata, US Patent 6,461,890, in view of Kaneda et al., US Patent 6,223,429, as applied to claim 41 above, and further in view of APA Figures 1-3.

Shibata fails to teach the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

APA teaches the chip contains a re-distributed line (RDL) pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the RDL of APA in the invention of Shibata because RDL patterns allow for greater flexibility and take advantage of unused chip space.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

David A. Zarneke
Primary Examiner
December 3, 2006